REMARKS

Claims 1-38 are pending.

Claims 1-38 are rejected.

Claims 35 and 36 have been amended to correctly depend from Claim 34. Claims 37 and 38 have been amended to correctly depend from Claim 36.

The Applicants respectfully assert that the amendments to Claims 35-38 and incorporated by reference in any claims depending therefrom, are not narrowing amendments made for a reason related to the statutory requirements for a patent that will give rise to prosecution history estoppel. *See Festo Corp. v. Shoketsu Kinzoku Kogyo Kabushiki Co.*, 122 S. Ct. 1831, 1839-40, 62 U.S.P.Q.2d 1705, 1711-12 (2002); 234 F.3d 555, 566, 56 U.S.P.Q.2d 1865, 1870 (Fed. Cir. 2001).

I. REJECTIONS UNDER 35 U.S.C. § 102

The Office Action rejected Claims 1, 3-8, 13, and 37 under *35 U.S.C. §102(b)* as being anticipated by U.S. Patent No. 6,240,485 to *Srinivasan* (hereafter "*Srinivasan*").

For a reference to anticipate a claimed invention, the reference must disclose every aspect of the claimed invention. *Verdegaal Bros. v. Union Oil Co. of California*, 814 F.2d 628, 631, 2 U.S.P.Q.2d 1051, 1053 (Fed. Cir. 1987). The identical invention must be shown in as complete detail as is contained in the claim. *Richardson v. Suzuki Motor Co.*, 868 F.2d 1226, 1236, 9 U.S.P.Q.2d 1913, 1920 (Fed. Cir. 1989).

Claim 1 recites a specific cooperative relationship between the first, second and third processing units using the first and second link inputs and the first and second link outputs. More specifically, Claim 1 recites a method of bi-directional communication between at least three adjacent processing units (first, second and third processing units). Each processing unit (first) being coupled to an upstream (second) processing unit and a downstream (third) processing unit. A logic state of a first enable signal determines

whether signals (third output signal) from the third processor on the second output link are coupled to the input of the first processing unit. Likewise, a logic state of the second enable signal determines if signals (first output signal) from the processing unit is coupled to the third processing unit on the second input link. Signals on the first output link from the first processing unit are coupled to gating logic in the second processing unit which determines whether or not to receive those signals at its input in response to an enabling signal. Likewise, second output signals from the second processing unit are coupled to the first processing unit on the first input link in response to enabling signals in the second processing unit. Each processing unit has gating logic that determines whether to send signals to or receive signals from its downstream processing unit. Likewise, signals to and from the upstream processing unit are coupled from its corresponding gating logic.

The Office Action states that *Srinivasan* teaches the invention of Claim 1 and cites FIG. 13 and its associated description. The invention of *Srinivasan* is directed to a content addressable memory (CAM) system wherein FIG. 13 shows three such CAM units 1302, 1304, and 1306.

The Office Action states that CAM units 1302, 1304, and 1306 are the first, second, and third processing units of Claim 1. The Office Action then refers to FIGS. 13, 15, and 16 as teaching a "cascade system for providing" the bi-directional communication bus recited in the pre-amble of Claim 6.

Claim 6 does not recite a cascade system but rather recites "a bi-directional communication bus in each of M processing units."

The Office Action does not identify the input and output of the first processing unit, the first and second link inputs and the first and second link outputs, or the first, second and third output signals as recited in Claim 1. The Office Action simply states (sic) "(e.g., see fig. 13)[links 1308, 1314, 1316 coupled outputs from a first processing unit 1302 via second processing unit 1304 to processing unit 1306 also using links 1318, 1324, 1326 using control signals 178, 138, and 140]." *Srinivasan* describes 1308 as a

"cascade down output" (/CSCDO) and that each CAM device may also provide a signal on its /CSCDO and /CSCUO pins indicating when the /MFDO (1314) and /MFUO (1312) flags are valid and may be sampled by the other CAMs. The match flags (MFDO 1314) indicate when comparand data on CBUS 138 matches the data in a CAM unit (e.g., 1302). Thus, 1308 and 1314 are not Link inputs or outputs as recited in Claim 1.

Element FFO 1316 cited by the Office Action is not described in detail and is referred to only as a "full flag output." Therefore, 1316 is not a Link inputs or outputs as recited in Claim 1

The Office Action states that 178, 138 and 140 are control signals. *Srinivasan* states that "CAM 100 is a synchronous CAM device that performs its operations in response to an external clock signal CLK 178." Therefore, CLK 178 is not a control signal as recited in Claim 1.

Srinivasan states that 138 is "a separate comparand bus CBUS 138 for receiving comparand data to be compared with one or more CAM cells." Therefore, CBUS 138 is not a control signal as recited in Claim 1.

Finally, *Srinivasan* states that 140 is an "IBUS 140 that is used to provide instructions to instruction decoder 128." Thus, IBUS 140 is not a control signal as recited in Claim 1.

In summary, Claims 1 and 6 recite enable signals and the Office Action erroneously states that signals 178, 138 and 140 are the enable signals of Claims 1 and 6 when in actuality they are a clock 178, a comparand bus 138, and an instruction bus 140.

The Office Action states that flag signals (e.g., /FFI 1316 and /MFDO 134) that indicate a status of the CAM units are the same as the first and second Link inputs and outputs recited in Claims 1 and 6. The status of one CAM is not coupled through a link to other CAMs. The signals /CSCDI, /CSCD, /MFUO, /MFUI, /FFI and /FFO do not form a bi-directional bus as recited in Claim 1 and 6 but are simply signals coupled from one adjacent CAM to another CAM unit. Instructions are coupled to each CAM on IBUS

140, comparand data is coupled to each CAM on CBUS 138 and when comparand data on the bus compares with the contents of one of the "content addressable memory" (CAM) units the associated data is outputted on ADS bus 142. FIG. 17 clearly shows that /CSCDO 1318 is a signal that is the logic combination of /CSCDI 1308 and CSCINT 136 and not a link as recited in Claims 1 and 6. FIG. 19 clearly shows that /MFDO 1324 is a signal that is the logic combination of /MFDI 1314 and MFINT 148 and not a link as recited in Claims 1 and 6. *Srinivasan* does not teach the bi-directional bus recited in Claim 6 or the method of communicating using a bi-directional bus recited in Claim 1.

Moreover, Claims 1 and 6 clearly describe the elements and their cooperative relationship. The Office Action does not identify which elements in *Srinivasan* specifically correspond to each element in Claims 1 and 6. The Office Action does not point out what is considered the output of the first processing unit (PU) or what is the first enable signal and fails to show how a first output signal is sent from the output of the first PU to the third PU on the second Link output or how a second output signal received on the first Link input from the second PU is selectively sent to the third PU on the second Link output in response to the first logic state of the first enable signal as recited in Claim 1 and 6. The Office Action does not point out what is the second enable signal and how a third output signal received on the second Link input from the third PU or the first output signal from the first PU is selectively sent to the second PU on the first Link output in response to the first logic state of the second enable signal. Finally, the Office Action does not point out what is considered the input of the first PU and how it receives the third output signal on the second Link input from the third PU or selectively receives the first output signal on the first Link input from the second PU when the first enable signal has the first logic state.

As a result of the foregoing, The Office Action has failed to show that *Srinivasan* discloses every aspect of Claims 1 and 6 and thus has failed to make a *prima facie* case of anticipation. Therefore, the Applicants assert that the rejections of Claim 1 and 6 under *35 U.S.C. §102(b)* as being anticipated by *Srinivasan* are traversed by the above arguments.

Claim 3 is dependent from Claim 1 and contains all the limitations of Claim 1. The Applicants have shown that *Srinivasan* does not anticipate Claim 1. Claim 3 adds the limitation that communication between the second PU and the first and third PU is blocked when the first and second enable signals concurrently have a second logic state. The Office Action states that *Srinivasan* teaches blocking of communication of data between processors when enabling signals were de-asserted, citing column 15, line 15 though column 16, line 67. CAM units 1302, 1304, and 1306 are coupled with buses IBUS 140, CBUS 138 and ADS bus 142. The second logic state of Claim 3 only has relevance when related to the first logic state that is operable to enable specific communication on the bi-directional bus of Claims 1 and 6. Claim 3 does not state any signal as being de-asserted. There is no discussion in this recitation of *Srinivasan* of blocking communication between the first, second and third processing units in response to enabling signals concurrently at a second logic state.

Therefore, the Applicants assert that the rejection of Claim 3 under *35 U.S.C. §102(b)* as being anticipated by *Srinivasan* is traversed by the above arguments and for the same reasons as Claim 1.

Claim 4 is dependent from Claim 1 and contains all the limitations of Claim 1. The Applicants have shown that *Srinivasan* does not anticipate Claim 1. Claim 4 adds the limitation that the second PU has a second Link output coupled to the first Link input of the first PU and a second Link input coupled to the first Link output of the first PU. The Applicants have shown that the Office Action did not point out what is considered the input and output of the CAM units of *Srinivasan*.

Therefore, the Applicants assert that the rejection of Claim 4 under *35 U.S.C. §102(b)* as being anticipated by *Srinivasan* is traversed by the above arguments and for the same reasons as Claim 1.

Claim 5 is dependent from Claim 1 and contains all the limitations of Claim 1. The Applicants have shown that *Srinivasan* does not anticipate Claim 1. Claim 5 adds the limitation that the third PU has a first Link input coupled to the second Link output of

the first PU and a first Link output coupled to the second Link input of the first PU. The Applicants have shown that the Office Action did not point out what is considered the input and output of the CAM units of *Srinivasan*.

Therefore, the Applicants assert that the rejection of Claim 5 under *35 U.S.C. §102(b)* as being anticipated by *Srinivasan* is traversed by the above arguments and for the same reasons as Claim 1.

Claim 7 is dependent from Claim 6 and contains all the limitations of Claim 6. The Applicants have shown that *Srinivasan* does not anticipate Claim 6. Claim 7 adds the limitation that the first Link input and a first function output from function logic circuitry are coupled to communication logic circuitry generating a first function output signal on the first Link output and a first communication output signal on a first communication output. What the Office Action states as corresponding to Links according to the present invention have been shown by the Applicants to be logic status signals. The Office Action states that *Srinivasan* teaches (sic) "function output from function logic (1502, 1618, FIGS. 15, 16) are coupled to communication logic circuitry (134) generating a first function output signal to the first link and a first communication output signal to a first communication output." Element 1502 is cascade logic generating the cascade signals and the flag signals. *Srinivasan* describes element 1618 as "cascade signal generator logic 1618." Element 134, which the Office Action states is communication logic circuitry, outputs to ADS BUS 142 and thus does not generate a first function output signal to the first Link output as recited in Claim 7.

Therefore, the Applicants assert that the rejection of Claim 7 under *35 U.S.C. §102(b)* as being anticipated by *Srinivasan* is traversed by the above arguments and for the same reasons as Claim 6.

The Office Action rejects Claim 37 for the same reason as Claim 7 even though Claim 37 recites different limitations from Claim 7. Therefore, the Applicants assert the Office Action fails to prove a *prima facie* case of anticipation since certain limitations in Claim 37 have not been addressed.

Claim 8 depends from Claim 7 and contains the same limitations of Claim 7. Claim 8 adds the limitation that the second Link input and the first communication output are coupled to the function logic circuitry generating a second function output signal on the first Link output and a second function output signal on a first function output. The Applicants have shown that *Srinivasan* does not anticipate Claims 6 or 7. The Office Action does not add anything material relative to Claim 8 and simply makes the assertion that FIGS. 13 and 15 show the limitations of Claim 8 without specifically pointing out which elements in these figures correspond to the elements recited in Claim 8.

Therefore, the Applicants assert that the rejection of Claim 8 under *35 U.S.C. §102(b)* as being anticipated by *Srinivasan* is traversed since the Office Action fails to prove a *prima facie* case of anticipation by not specifically showing how the prior art anticipates Claim 8.

Claim 13 is dependent from Claim 7 and contains all the limitations of Claim 7. Claim adds the limitation that the input of the first PU is coupled to the first function output of the function logic circuit. The Applicants have shown that *Srinivasan* does not anticipate Claim 7. The Applicants have also shown that the Office Action does not point out what element in *Srinivasan* is considered the input of the first PU. The Applicants have pointed out that the most logically the input to the CAMs are either the IBUS 140 or the CBUS 138 neither of which are coupled to the first function output of the function logic circuit of Claim 13.

Therefore, the Applicants assert that the rejection of Claim 13 under *35 U.S.C. §102(b)* as being anticipated by *Srinivasan* is traversed for the same reasons as Claims 6 and 7.

II. REJECTIONS UNDER 35 U.S.C. § 103

To establish a *prima facie* case of obviousness, the Office Action must meet three basic criteria. First, there must be some suggestion or motivation, either in the references

themselves or in the knowledge generally available to one of ordinary skill in the art, to modify the reference or to combine reference teachings. Second, there must be some reasonable expectation of success. Finally, the prior art reference must teach or suggest all the claim limitations.

The Office Action rejected Claims 17-19 under *35 U.S.C. § 103(a)* as being unpatentable over *Srinivasan* in view of U.S. Patent No. 5,831,997 to *Kodashiro* (hereafter "*Kodashiro*").

Claim 17 is dependent form Claim 6 and contains all the limitations of Claim 6. Claim 17 adds the limitation that the first and second PUs are pattern detection processing units, each for comparing an input data byte to a pattern byte selected for a sequence of pattern bytes stored in each of the first and second PUs and generating a compare output in each of the first and second PUs, wherein the pattern byte in each of the PUs is selected by an address pointer and modified in response to a logic state of the compare output and an operation code stored with the selected pattern byte.

The Applicants have shown that *Srinivasan* does not anticipate Claim 6. The Office Action admits that *Srinivasan* does not teach that the pattern byte in each of the PUs is modified in response to a logic state of the compare output and an operation code stored with the selected pattern byte.

For a reference or combination of references to teach or suggest Claim 17 then all the limitations of Claim 17 must be in the references and their must be some motivation to combine the teachings of the references including an expectation that the combination would be successful. The Office Action states that "*Kodashiro* teaches modifying a pattern in response to a compare output (selector output that indicates a tester model using the test pattern) and operation code stored in memory." The Office Action cites *Kodashiro* column 1, lines 7-67 and column 2, line 25 through column 3, line 35.

The Applicant searched the disclosure of *Kodashiro*. *Kodashiro* describes a pattern generation apparatus and not a pattern matching processing unit. Pattern

generation is not even in the same field as pattern matching. There would be no motivation for one configuring a bi-directional communication bus coupling a plurality of pattern matching processing units to look to *Kodashiro*. Secondly, teachings attributed to *Kodashiro* by the Office Action could not be found by the Applicant. The Applicant does not see any relevance to the present invention in modifying a pattern in a tester based on the tester model as stated by the Office Action. The present invention is directed to providing a specific type of bi-directional communication bus between processing units and in particular, according to Claim 17, when those processing units are pattern matching processing units. Claim 17 is not directed to generating a pattern from an instruction and test data. The Applicant does not see any relevance to the Office Actions assertion that one would combine the teachings of *Srinivasan* directed to a content addressable memory system with *Kodashiro* generating test patterns to arrive at a method of forming a bi-direction communication bus for coupling between parallel pattern matching processors. The Applicants assert that neither *Srinivasan* and *Kodashiro* singly or in combination teach or suggest the invention of Claim 17.

Therefore, the Applicants assert that the rejection of Claim 17 under *35 U.S.C. §103(a)* as being obvious over *Srinivasan* in view of *Kodashiro* is traversed by the above arguments.

Claim 18 is dependent from Claim 17 and contains all the limitations of Claim 17. The Applicants have shown that neither *Srinivasan* and *Kodashiro* singly or in combination teach or suggest the invention of Claim 17. Claim 18 adds the limitation that the bi-directional communication between the first PU and the second PU is enabled to allow increment signals from the first and second PU, for incrementing their respective address pointers, to be coupled to and logic combined in the control logic of the first PU and control logic of the second PUs to generate a modified increment address pointer signal at the PU input of the first PU and the one or more adjacent PUs. The Office Action states that *Srinivasan* alone teaches the limitation of Claim 18. The Office Action states that since *Srinivasan* shows a next free address element 106, that it necessarily follows that one of ordinary skill in the art would arrive at the invention of Claim 18.

Srinivasan states that next free addresses are obtained from next free address register 106 and that the next free address corresponds to the next available address that may be written to in CAM array 104. Claim 18 is directed to functionality of the bi-directional bus and not to the functionality of an address used to access data. The bi-directional bus of Claim 17 is enabled to allow increment signals to be communicated between processing units for a specific purpose. The Applicant therefore asserts that *Srinivasan* only discusses obtaining the next free address from element 106 and does not discuss enabling the bi-directional bus of Claim 17 to communicate increment signals between processing units to modify and address pointer.

Therefore, the Applicants assert that the rejection of Claim 18 under *35 U.S.C. §103(a)* as being obvious over *Srinivasan* in view of *Kodashiro* is traversed by the above arguments and for the same reasons as Claim 17.

Claim 19 is dependent from Claim 18 and contains all the limitations of Claim 18. The Applicants have shown that neither *Srinivasan* and *Kodashiro* singly or in combination teach or suggest the invention of Claim 18. Claim 19 adds the limitation that the modified increment address pointer signal is used to enable advanced matching capabilities to be performed by the first and second PU by incrementing the address pointer in the first PU or the second PU if either the first or second PU generates a logic state on its corresponding compare output indicating that a particular input data byte has compared to either selected pattern byte in the first or second PU. The Office Action does not specifically address Claim 19 but rather rejects Claim 19 for the same reasons as Claim 18 even though Claim 19 has more limitations than Claim 18.

The Applicants assert that the Office Action fails to make a *prima facie* case of obviousness for Claim 19. Therefore, the Applicant further asserts that the rejection of Claim 19 under *35 U.S.C. §103(a)* as being obvious over *Srinivasan* in view of *Kodashiro* is traversed by the above arguments and for the same reasons as Claim 18.

The Office Action rejected Claims 2, 9-12, 14-16, and 35-36 under *35 U.S.C. § 103(a)* as being unpatentable over *Srinivasan* in view of U.S. Patent No. 6,127,849 to *Walker* (hereafter "*Walker*").

Claim 2 is dependent from Claim 1 and contains all the limitations of Claim 1. Claim 2 adds the limitation that the specific first and second enable signals of Claim 1 are generated by control logic in the first PU. The Applicants have shown that *Srinivasan* does not anticipate Claim 1 and the Office Action makes no assertion that *Srinivasan* teaches or suggest the invention of Claim 2. The first and second enable signals determine whether bi-directional communication is enabled between the first and third processing units on the Link in and Link out connections. The Office Action states that *Srinivasan* anticipates the limitations of Claim 1 and *Walker* teaches the limitations of Claim 2 and thus it would have been obvious to combine the two teachings to arrive at the invention of Claim 2.

Walker teaches a method of simultaneous bi-directional communication over a single wire; this is totally different from bi-directional communication over a Link in and a Link out connection. Since *Walker* sends and receives over the same node, there is no separate enable for the Link in and Link out, *Walker* would have only one enable signal which would determine send and receive. The Applicants assert there would be no motivation to incorporate the teachings of *Walker* into *Srinivasan* since *Srinivasan* is directed to CAM systems with standard buses and *Walker* is directed to simultaneous bi-directional buses using a single line to transmit and receive. *Walker* can disable or enable communication but *Walker* cannot separately enable transmit while disabling receive which is possible with first and second enable signals of Claim 2. Claim 2 recites an invention that allows self-contained processing units to be added in parallel wherein all of the control logic necessary for enabling communication to its adjacent processor is contained in the added processing unit and only the links to the downstream processor need be connected. *Srinivasan* and *Walker* teach dissimilar systems whose teachings cannot be combined to arrive at the invention of Claim 2.

Therefore, the Applicant further asserts that the rejection of Claim 2 under *35 U.S.C. §103(a)* as being obvious over *Srinivasan* in view of *Walker* is traversed by the above arguments and for the same reasons as Claim 1.

The Office Action states that Claims 9-12, 14-16 and 35-36 are "directed to the implementation of the enabling function and communication input/output using gates and signals." Claims 9-12 recite details of the bi-directional bus of Claims 6-8. The bi-directional bus allows processing units to be added in parallel wherein control of the bus for added processing units is contained in the added processing unit.

Claims 9-12 and 14-15 depend indirectly depend from Claim 6 and thus contain all the limitations of Claim 6. The Applicants have shown that Claim 6 is not anticipated by *Srinivasan*. The Office Action does not state that *Walker* teaches anything relative to Claim 6. Therefore the Office Action relies on *Walker* to teach the limitations of Claims 9-12 and 14-15 not contained in Claim 6. The invention of *Walker* is directed to simultaneous bi-directional communication over a single line between two communicating units and the Applicants assert that it cannot be shown that *Walker* generally applies to the claims of the present invention as is assumed by the present Office Action. The Applicants assert that the Office Action has confused being able to simultaneously receive on one Link and transmit on a second Link with *Walker's* "simultaneous bi-directional communication" over a single wire. The particular logic described in Claims 9-12 and the teachings of *Walker* are totally different. The Applicants assert the Office Action has failed to make a *prima facie* case of obviousness by broadly stating that the invention of *Srinivasan*, directed to CAM systems and *Walker* directed to single wire simultaneous bi-directional communication, teach Claims 9-12, 14, 15, 35 and 36.

Therefore the Applicants assert that the rejections of Claims 9-12, 14-15 and 34-35 under *35 U.S.C. §103(a)* as being obvious over *Srinivasan* in view of *Walker* are traversed by the above arguments and for the same reasons as Claim 6.

The Office Action rejected Claims 20-29 under *35 U.S.C. § 103(a)* as being unpatentable over *Srinivasan* in view of U.S. Patent No. 5,787,200 to *Sceiza* (hereafter "*Sceiza*").

Claims 20-29 are directed to a data processing system that has one or more parallel pattern detection engines (PPDEs each with an input/output (I/O) interface including the bidirectional bus described in Claims 6-15. The Office Action repeats the arguments cited for Claims 1 and 6 stating that *Srinivasan* anticipates both the method of Claim 1 and the bi-directional bus of Claim 6. Since Claims 20-29 further include the limitations of data processing elements recited in Claim 20, the Office Action states that *Srinivasan* does not teach this limitation. The Office Action states that *Sceiza* teaches the data processing limitations of Claim 20 and that it would have been obvious to combine the teachings of *Sceiza* and *Srinivasan* to arrive at the inventions in Claims 20-29. The Office Action states that *Sceiza* teaches a "character pattern recognition system comprising a (master processor), RAM and that *Srinivasan* teaches CAM with LEARN instructions for detecting patterns."

The Applicants have shown that *Srinivasan* does not teach or suggest the bi-directional bus recited in Claim 6. The Office Action relies on *Srinivasan* only as teaching a character pattern recognition system comprising a (master processor) and RAM. One of ordinary skill in the art cannot combine the teachings of *Srinivasan* and *Sceiza* to arrive the inventions of Claims 20-29. The Office Action states that the addition of *Sceiza* would have provided *Srinivasan* a means to receive control commands and data and a place to store output data. This has nothing to do with the bi-directional bus of Claim 6 incorporated into a data processing system as recited in Claims 20-29. Claim 21 is rejected over *Srinivasan* for the same reasons as Claim 7 which the Applicants have traversed. Claim 22 is rejected over *Srinivasan* for the same reasons as Claim 8 which the Applicants have traversed. Claim 27 is rejected over *Srinivasan* for the same reasons as Claim 13 which the Applicants have traversed. Claims 23-26, and 28-29 are rejected over *Srinivasan* for the same reasons as Claims 9-12 and 14-15.

The Applicants assert that the Office Action has failed to make a *prima facie* case of obviousness for Claim 20-29. There is no motivation to combine a CAM system with a character pattern recognition system to arrive at the data processing system of Claim 20. The Applicants have shown that *Srinivasan* does not teach or suggest the bi-directional communication bus of Claims 6 incorporated into Claim 20. The Office Action is silent regarding teachings of *Sceiza* relative to the bi-directional communication bus of Claims 6 incorporated into Claim 20, thus there would be not expectation that combining the two references would lead to the inventions of Claims 20-29. Finally, there has been no showing that the combination of *Srinivasan* and *Sceiza* teach or suggest all the elements of Claims 20-29.

Therefore the Applicants assert that the rejections of Claims 20-29 under *35 U.S.C. §103(a)* as being obvious over *Srinivasan* in view of *Sceiza* are traversed by the above arguments and for the same reasons as Claim 6.

The Office Action rejected Claims 31-33 under *35 U.S.C. § 103(a)* as being unpatentable over *Srinivasan* in view of *Sceiza* and further in view of *Kodashiro*.

Claims 31-33 are directed to a data processing system that contains the limitations of Claim 6. In rejecting Claims 31-33 the Office Action uses the exact same argument used to reject Claim 17-19 over *Srinivasan* in view of *Kodashiro*. As to the teachings of *Sceiza* relative to Claim 31-33, the Office Action is silent. The Applicants assert that the Office Action has failed to make a *prima facie* case of obviousness for Claim 31-33 over *Srinivasan* in view of *Sceiza* and further in view of *Kodashiro*.

Therefore the Applicants assert that the rejections of Claims 31-33 under *35 U.S.C. §103(a)* as being obvious over *Srinivasan* in view of *Sceiza* and further in view of *Kodashiro* are traversed by the above arguments and for the same reasons as Claims 17-19.

The Office Action rejected Claim 30 under *35 U.S.C. § 103(a)* as being unpatentable over *Srinivasan* in view of *Sceiza* and further in view of *Walker*.

Claim 30 is directed to a data processing system that contains the limitations of Claim 6. In rejecting Claim 30 the Office Action uses the exact same argument used to reject Claims 2 and 16 over *Srinivasan* in view of *Walker*. As to the teachings of *Sceiza* relative to Claim 30, the Office Action is silent. The Applicants assert that the Office Action has failed to make a *prima facie* case of obviousness for Claim 30 over *Srinivasan* in view of *Sceiza* and further in view of *Walker*.

Therefore the Applicants assert that the rejections of Claim 30 under *35 U.S.C. §103(a)* as being obvious over *Srinivasan* in view of *Sceiza* and further in view of *Walker* are traversed by the above arguments and for the same reasons as Claims 2 and 16.

The Office Action rejected Claim 34 under *35 U.S.C. § 103(a)* as being unpatentable over *Srinivasan* in view of *Walker*.

Claim 34 is an independent claim to a processing unit and not a data processing system (DP). The Office Action rejected Claim 34 for essentially the same reasons a Claim 20. Claim 34 recites different limitations than Claim 20. The Office action fails to make a *prima facie* case of obviousness for failing to address each of the elements of Claim 34. Instead, the Office Action relies on broad statements that do not specifically point out in the cited references where the elements of Claim 34 and their cooperative relationship are found in *Srinivasan* and *Walker*.

Therefore the Applicants assert that the rejections of Claim 34 under *35 U.S.C. §103(a)* as being obvious over *Srinivasan* in view of *Walker* are traversed by the above arguments and for the same reasons as Claim 20.

The Office Action rejected Claim 38 under *35 U.S.C. § 103(a)* as being unpatentable over *Srinivasan* in view of *Kodashiro*.

Claim 38 is dependent from Claim 36 and contains all the limitations of Claim 36. The Office Action rejected Claim 38 for essentially the same reasons as Claim 17 even though Claim 38 has different limitations that Claim 17. The Applicants assert that

the Office Action has failed to make a *prima facie* case of obviousness for Claim 38 over *Srinivasan* in view of *Kodashiro* for failing to address all the limitations of Claim 38.

Therefore the Applicants assert that the rejections of Claim 38 under *35 U.S.C. §103(a)* as being obvious over *Srinivasan* in view of *Kodashiro* are traversed by the above arguments and for the same reasons as Claim 17.

III. CONCLUSION

Claims 35-38 have been amended to correct dependencies and thus remove antecedent basis problems.

The rejections of Claims 1, 3-8, 13, and 37 under *35 U.S.C. §102(b)* as being anticipated by *Srinivasan* have been traversed.

The rejections of Claims 17-19 under *35 U.S.C. § 103(a)* as being unpatentable over *Srinivasan* in view of *Kodashiro* have been traversed.

The rejections of Claims 2, 9-12, 14-16, and 35-36 under *35 U.S.C. § 103(a)* as being unpatentable over *Srinivasan* in view of *Walker* have been traversed.

The rejections of Claims 20-29 under *35 U.S.C. § 103(a)* as being unpatentable over *Srinivasan* in view of *Sceiza* have been traversed.

The rejections of Claims 31-33 under *35 U.S.C. § 103(a)* as being unpatentable over *Srinivasan* in view of *Sceiza* and further in view of *Kodashiro* have been traversed.

The rejection of Claim 34 under *35 U.S.C. § 103(a)* as being unpatentable over *Srinivasan* in view of *Walker* has been traversed.

The rejection of Claim 38 under *35 U.S.C. § 103(a)* as being unpatentable over *Srinivasan* in view of *Kodashiro* has been traversed.

The Applicant, therefore, respectfully asserts that Claims 1-38 are also now in condition for allowance and requests an early allowance of these claims.

Applicants respectfully request that the Office Action call Applicant's attorney at the below listed number if the Office Action believes that such a discussion would be helpful in resolving any remaining problems.

Respectfully submitted,

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